PATENT CLAIMS

1. A method of driving a passive matrix addressed display or memory array of cells comprising an electrically polarizable material exhibiting hysteresis, in particular a ferroelectric material, wherein the polarization state of individual, separately selectable cells can be switched to a desired condition by application of electric potentials or voltages to word and bit lines in said matrix, and wherein the method is
characterized by
controlling individually a potential on selected word and bit lines to approach or coincide with one of n predefined potential levels, where $n \geq 3$, the potentials on said selected word and bit lines forming subsets of said n potentials involving n_{WORD} and n_{BIT} potentials, respectively;
controlling the potentials on all word- and bit lines in a time-coordinated fashion according to a protocol or timing sequence, whereby word lines are latched in a predetermined sequence to potentials selected among the n_{WORD} potentials, while bit lines are either latched in a predetermined sequence to potentials selected among the n_{BIT} potentials or they are during a certain period of the timing sequence connected to circuitry that senses the charges flowing between the bit line(s) and the cells connecting to said bit line(s); and
arranging said timing sequence to encompass at least two distinct parts, including a "read cycle" during which charges flowing between said selected bit line(s) and the cells connecting to said bit line(s) are sensed, and a "refresh/write cycle" during which polarization state(s) in cells connecting with selected word- and bit lines are brought to correspond with a set of predetermined values.

2. A method according to claim 1,
characterized by allowing one or more bit lines to float in response to charges flowing between the bit line and the cells connecting to said bit line during said read cycle, and clamping all voltages on the word and bit lines during the refresh/write cycle.

3. A method according to claim 1,
characterized by selecting the values $n = 3$ and $n_{WORD} = 3$ and $n_{BIT} = 3$, in case the voltages across non-addressed cells do not significantly exceed $V_S/2$,

where V_S is the voltage across the addressed cell during read, refresh and write cycles.

4. A method according to claim 1,
characterized by selecting the values n = 4 and n_{WORD} = 4 and n_{BIT} = 4, in case the voltages across non-addressed cells do not significantly exceed $V_S/3$, where V_S is the voltage across the addressed cell during read, refresh and write cycles.

5. A method according to claim 1,
characterized by selecting the values n = 5 and n_{WORD} = 3 and n_{BIT} = 3, in case the voltages across non-addressed cells do not significantly exceed $V_S/3$, where V_S is the voltage across the addressed cell during read, refresh and write cycles.

6. A method according to claim 1,
characterized by subjecting non-addressed cells along an active word line and along active bit line(s) to a maximum voltage during the read/write cycle that deviates by a controlled value from the exact values $V_S/2$ or $V_S/3$.

7. A method according to claim 6,
characterized by subjecting non-addressed cells along an active word line to a voltage of a magnitude that exceeds the exact values $V_S/2$ or $V_S/3$ by a controlled voltage increment, and at the same time subjecting non-addressed cells along selected active bit lines to a voltage of a magnitude that is less than the exact values $V_S/2$ or $V_S/3$ by a controlled voltage decrement.

8. A method according to claim 8,
characterized by the controlled voltage increment and voltage decrement being equal to each other.

9. A method according to claim 1,
characterized by adding a controlled voltage increment $\delta 1$ to the potentials $\Phi_{inactive}$WL of inactive word lines and adding a controlled voltage increment $\delta 2$ to the potentials $\Phi_{inactive}$BL of inactive bit lines, where $\delta 1 = \delta 2 = 0$ corresponds to the read/write protocols with maximum $V_S/2$ or $V_S/3$ voltage exposure on non-selected cells.

10. A method according to claim 9,
characterized by $\delta_1 = \delta_2 \neq 0$.

11. A method according to claim 1,
characterized by controlling a quiescent potential (the potential imposed on the word and bit lines during the time between each time the read/refresh/write cycle protocol is employed) to have the same value on all word- and bit lines, i.e. a zero voltage is imposed on all cells.

12. A method according to claim 1,
characterized by selecting quiescent potentials on one or more of the word- and bit lines among one of the following: a) System ground, b) Addressed word line at initiation of pulsing protocol, c) Addressed bit line at initiation of pulsing protocol, d) Power supply voltage (V_{CC}).

13. A method according to claim 1,
characterized by selecting the potential on the selected bit line(s) in a quiescent state such that it differs from that at the onset of a floating period (read cycle), and by said potential being brought from a quiescent value to that at the onset of the floating period, where it is clamped for a period of time comparable to or exceeding a time constant for charging the bit line ("pre-charge pulse").

14. A method according to claim 1,
characterized by preceding the read cycle with a voltage shift on inactive word lines, whereby the non-addressed cells on an active bit line are subjected to a voltage bias equal to that occurring due to the active bit line voltage shift during the read cycle, said voltage shift on the inactive word lines starting at a selected time preceding said voltage shift on the active bit line, and terminating at the time when the latter voltage shift is initiated, in such a way that a perceived voltage bias on said non-addressed cells on the active bit line is continuously applied from the time of initiation of said voltage shift on the inactive word lines and up to the time of termination of said voltage shift on the active bit lines ("pre-charge pulse").

15. A method according to claim 1,
characterized by applying a pre-read reference cycle which precedes the read cycle and is separated from it by a selected time, and which mimics precisely the pulse protocol and current detection of said read cycle, with the exception

that no voltage shift is imposed on an active word line during said pre-read reference cycle, and by employing a signal recorded during said pre-read reference cycle as input data to the circuitry that determines the logic state of the addressed cell.

16. A method according to claim 15, characterized by said signal recorded during the pre-read cycle being subtracted from a signal recorded during the read cycle.